

REMARKS

Claims 1-21 are pending in this application. Claims 1, 2, 3, 6, 7, 13, 15 and 19 are amended.

Favorable reconsideration of this application, in light of the following remarks and amendments, is respectfully requested.

Entrance of the amendments to the claims is respectfully requested, because the amendments place the claims in a condition for allowance. In addition, matters added to independent claims 1 and 13 have already been considered by the Examiner (additional comments below). Minor amendments to dependent claims 2, 3, 6, and 15 are made to correct antecedent basis problems. Amendments to claims 7 and 19 are made to place the claims into proper dependent form.

Rejections under 35 U.S.C. §102

Claims 1-21 stand rejected under 35 U.S.C. §102(b) as being anticipated by Emer et al. (U.S. Patent No. 6,073,159). The Applicants respectfully traverse this rejection for the reasons detailed below.

In the Examiner response to Applicants' remark, the Examiner opines:

The fetch unit selects from among multiple program counters (i.e. threads) instructions to fetch (column 3, lines 62-67). This selection is done responsive to thread attributes information collected for each thread (column 6, lines 22-45). This thread attribute information comes from other stages. For example, under the BRCOUNT selection scheme, the number of branch instructions in the decode, rename, and queue stages are counted (column 7, lines 51-64). In order for the number of branches within a particular stage to be counted, branches must be counted during, or within, that particular stage. Since this counting is done in the above-mentioned stages, thread attribute information is received from these stages.

With all due respect, in the quoted passage above, the Examiner reiterates what Applicants have already disclosed in the present application. See paragraph [0006]. Paragraph [0006] discloses the prior art, USP 6,470,443, which is a divisional of USP 6,073,159. The present application also discloses that the SMT processor of '443 and '159 fail to consider an operation cycle account.

Accordingly, Applicants have amended independent claims 1 and 13 to recite, *inter alia*, that a fetch unit generates a weighted instruction count for each thread, which “is a count of the instructions for the thread with each instruction weighted by cycle counts associated with processing the instruction.” (Emphasis added.)

The Examiner will note that the quoted recitation above is similar to the recitation in original claims 7 and 19. With regard to claims 7 and 19, the Examiner alleges that column 13, line 66 to column 14, line 26 teach “the weighted instruction count for a thread is a count of the instructions for the thread in the processing pipeline with each instructions weighted by the cycle counts [*constants C_n*] associated with processing the instruction.” (Emphasis added.)

As the Examiner may be aware, “cycle count” refers to cycle count values of system clocks, which means that cycle counts are dynamic. The '159 reference specifically teaches that **constant** C_n “represents the apparent value of each fetching scheme in reference to each other.” Accordingly, **constant** C_n is not the same thing as cycle counts.

For at least the reasons given above, claim 1 is patentable over the cited reference. Similarly recited independent claim 13 is also patentable for the same reasons given above with respect to the patentability of claim 1.

Claims 2-12 and 14-21, dependent on independent claims 1 and 13, respectively, are patentable for the reasons stated above with respect to claims 1 and 13 as well as for their own merits.

Also in view of the comments made above, Applicants request entrance of the amendments to claims 1 and 13, because the merit of the subject matter of claims 7 and 19 have been consider by the Examiner and the amendment places the claims in a condition for allowance.

Rejections under 35 U.S.C. §102

Claims 1 and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Borkenhagen et al. (U.S. Patent No. 6,073,159). The Applicants respectfully traverse this rejection for the reasons detailed below.

Applicants note that only claims 1 and 13 are rejected as being anticipated by Borkenhagen et al., which means the subject matter of claim 7, for example, is patentable over Borkenhagen et al. As remarked above, the subject matter of claim 7 has been incorporated into independent claims 1 and 13.

Accordingly, claims 1 and 13 are patentable over Borkenhagen et al.

CONCLUSION

In view of the above remarks and amendments, the Applicants respectfully submit that each of the pending objections and rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

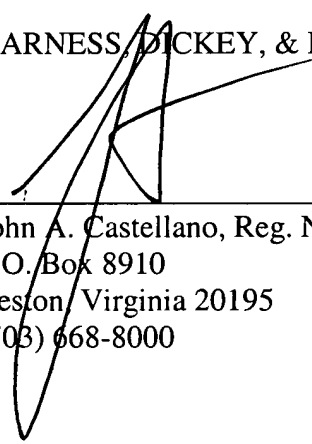
Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKY, & PIERCE, P.L.C.

By



John A. Castellano, Reg. No. 35,094
P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/LYP/tlt